average. In Table 1, this corresponds to limiting the rows to those designated as having four 5 ms slots. There is one such row for each encoder packet size. The encoder packet size is then selected, indexed by the T/P value. The remainder of the parameters, such as repetition factor, modulation format, Walsh channel selection, code rate, and so forth, are given in the appropriate row. Those of skill in the art will readily extend this to myriad sets of channel parameters, in addition to those shown in Table 1.

In step **1750**, lower latency is desired, so fewer than the maximum number of subpackets are selected for the expected number of subpacket retransmissions (the actual number of retransmissions will vary, depending on the channel conditions, probability of error, etc.). For the lowest latency possible, the mobile station may select a row such that the expectation (to within a desired probability) is of successful transmission in a single subpacket. Of course, if the data to be transmitted does not fit in a single subpacket, given the available T/P, actual latency may be reduced by selecting a row with more than one subpacket (i.e. 2 or 3). Note that the base station may be able to reallocate subpackets not used by the mobile station (i.e. a decision is made to use fewer than the maximum). In the example embodiment, the T/P grant is made assuming the mobile station has the right to use all the subpackets. If an earlier subpacket is received correctly, the base station may ACK-and-Continue (if additional data is awaiting transmission), or reallocate the subsequent ARQ channel slots to a different mobile station. Again, too much latitude afforded to the mobile station may result in less tight control over the RoT, and thus potential throughput losses. Those of skill in the art will fine tune the flexibility for the desired system performance.

Various methods for selecting the row from a table of possible combinations will be apparent to those of skill in the art, in light of the teachings herein. One example is to order the table based on the required T/P for each combination of data rate (and other parameters) and expected number of subpackets. The mobile station would then choose the combination with the features desired (latency, throughput, etc.) from the subset supportable by the given T/P. Or, more simply, the T/P may be an index to a specific row. The indexed row may be updated through signaling. If additional flexibility is desired, the number of subpackets chosen may be indexed for the given T/P. Certain data types, such as FTP, for example, may always select the maximum throughput option (i.e. maximum encoder packet size with largest expected number of subpacket retransmissions).

Again, this example is described using the example T/P system allocation parameter. Alternate embodiments may use an alternate parameter, or may specifically direct one or more of the parameters for use by the mobile station. From either step **1740** or **1750**, once the parameters have been selected, the process may stop.

It should be noted that in all the embodiments described above, method steps can be interchanged without departing from the scope of the invention. The descriptions disclosed herein have in many cases referred to signals, parameters, and procedures associated with the 1xEV-DV standard, but the scope of the present invention is not limited as such. Those of skill in the art will readily apply the principles herein to various other communication systems. These and other modifications will be apparent to those of ordinary skill in the art.

Those of skill in the art will understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

Those of skill will further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A method of transmission, comprising:

storing data in a data buffer at a mobile station;

transmitting an access request message;

monitoring a plurality of grant channels, the plurality of grant channels including one or more individual grant channels and one or more common grant channels;